FIG. 1

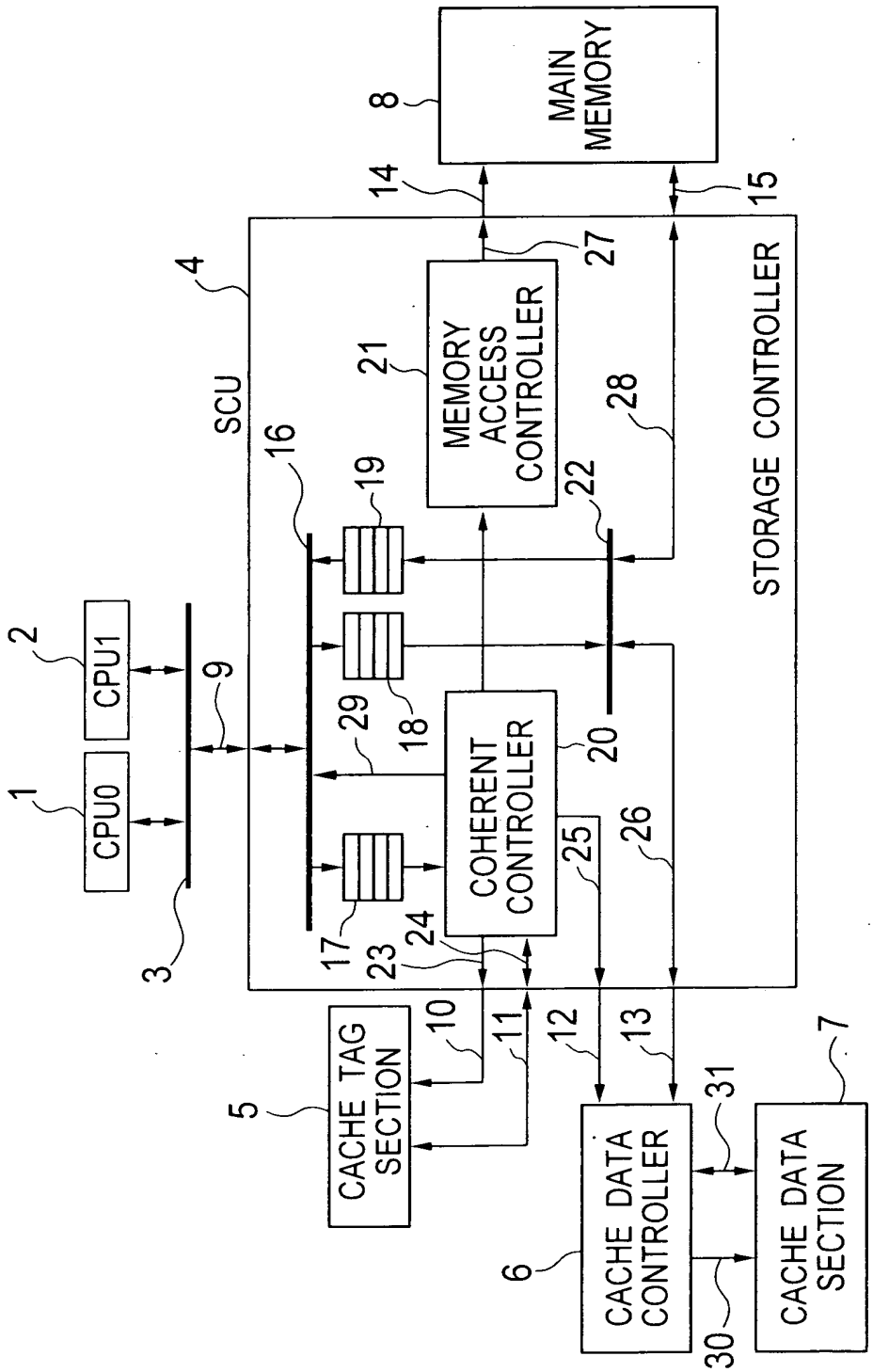

CPU0
CPU1
MAIN MEMORY
SCU
STORAGE CONTROLLER
MEMORY ACCESS CONTROLLER
COHERENT CONTROLLER
CACHE TAG SECTION
CACHE DATA CONTROLLER
CACHE DATA SECTION
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31

FIG. 2

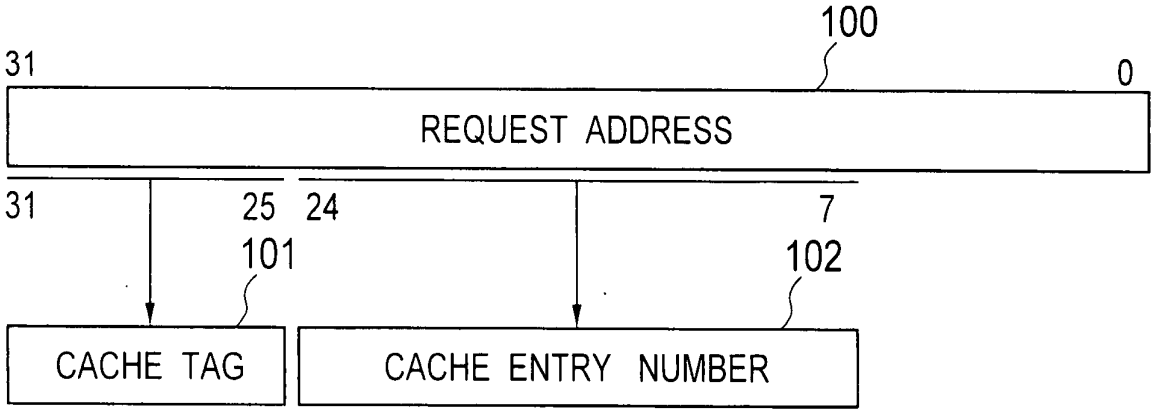

100
31
0
REQUEST ADDRESS
31
25
24
7
101
102
CACHE TAG
CACHE ENTRY NUMBER

FIG. 3

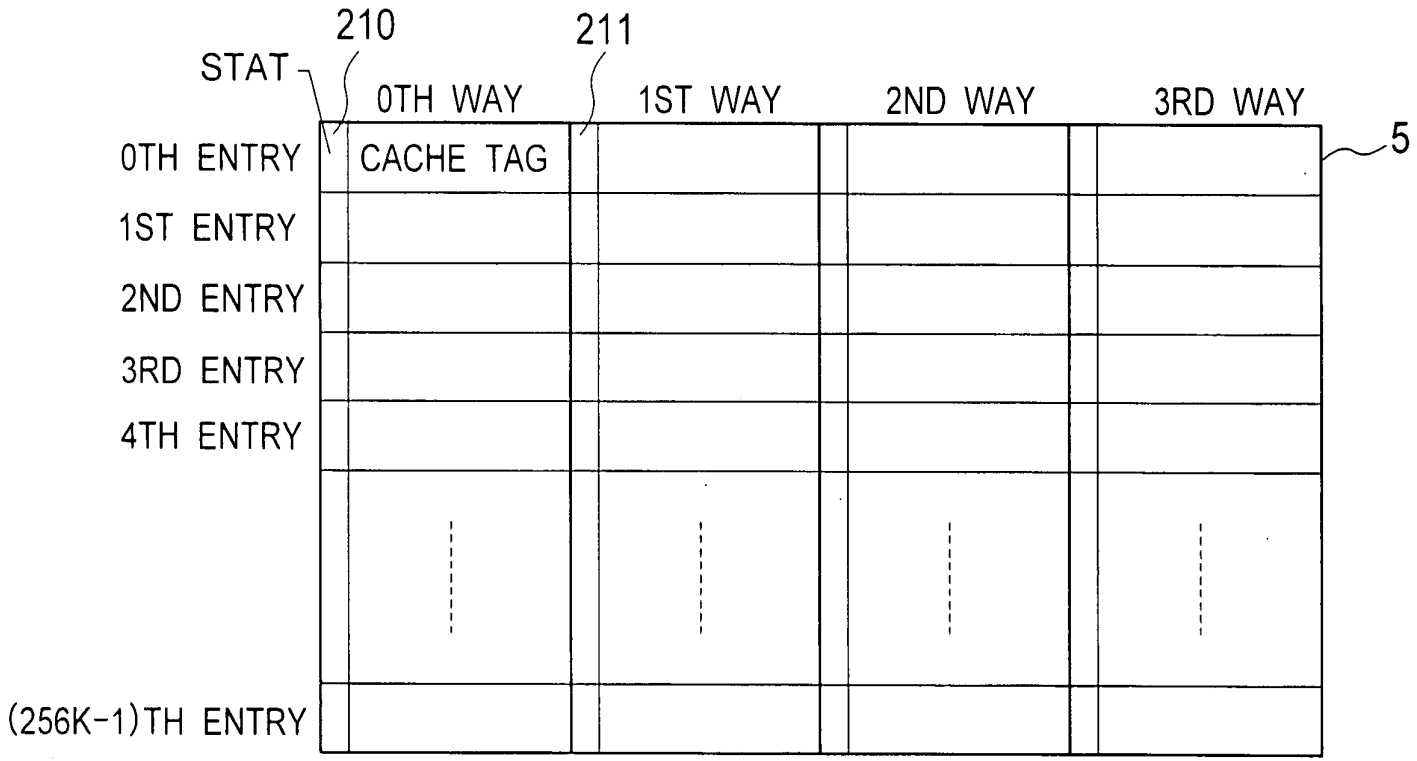

210
211
STAT
0TH WAY
1ST WAY
2ND WAY
3RD WAY
0TH ENTRY
CACHE TAG
1ST ENTRY
2ND ENTRY
3RD ENTRY
4TH ENTRY
(256K-1)TH ENTRY
5

FIG. 4

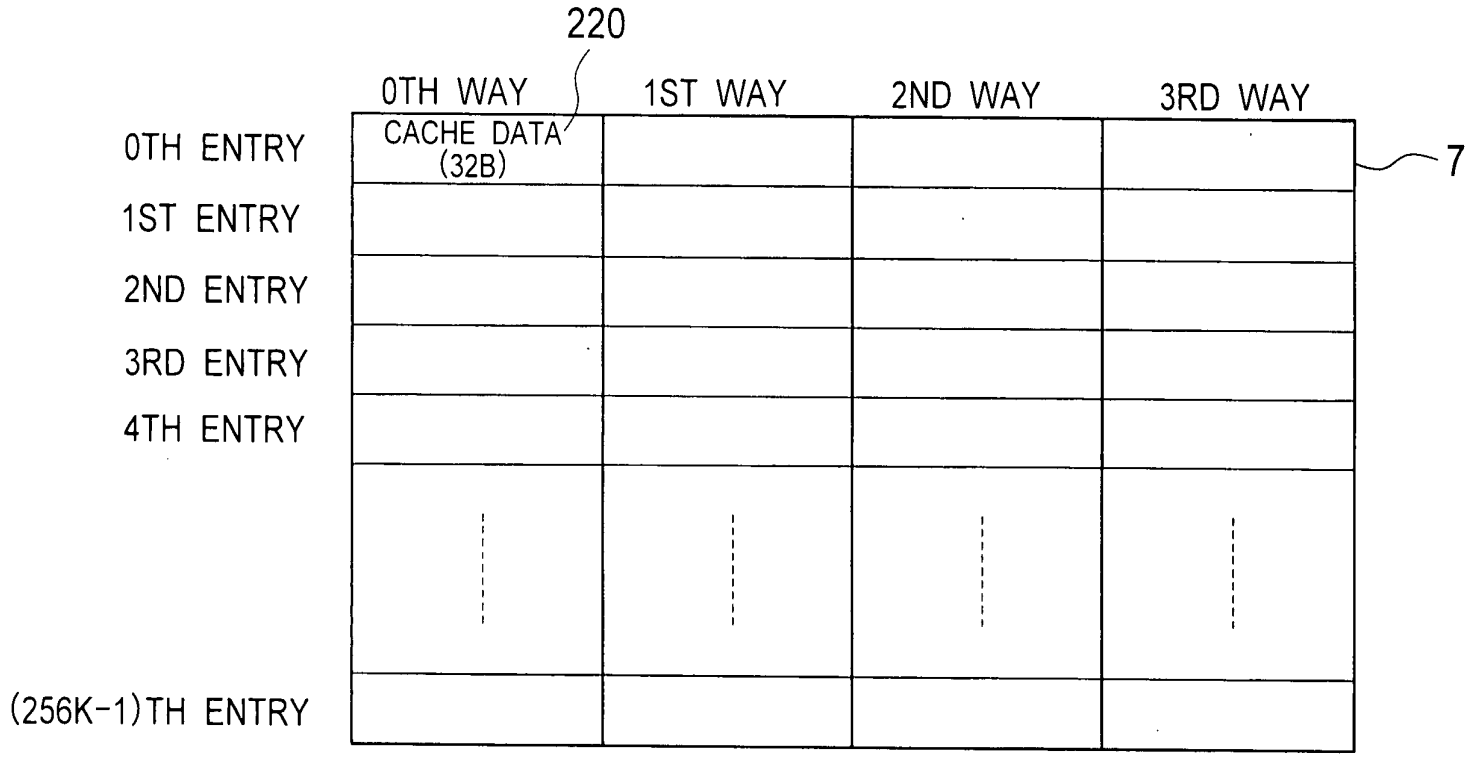

220
0TH WAY
1ST WAY
2ND WAY
3RD WAY
0TH ENTRY
CACHE DATA (32B)
1ST ENTRY
2ND ENTRY
3RD ENTRY
4TH ENTRY
(256K-1)TH ENTRY
7

FIG. 5

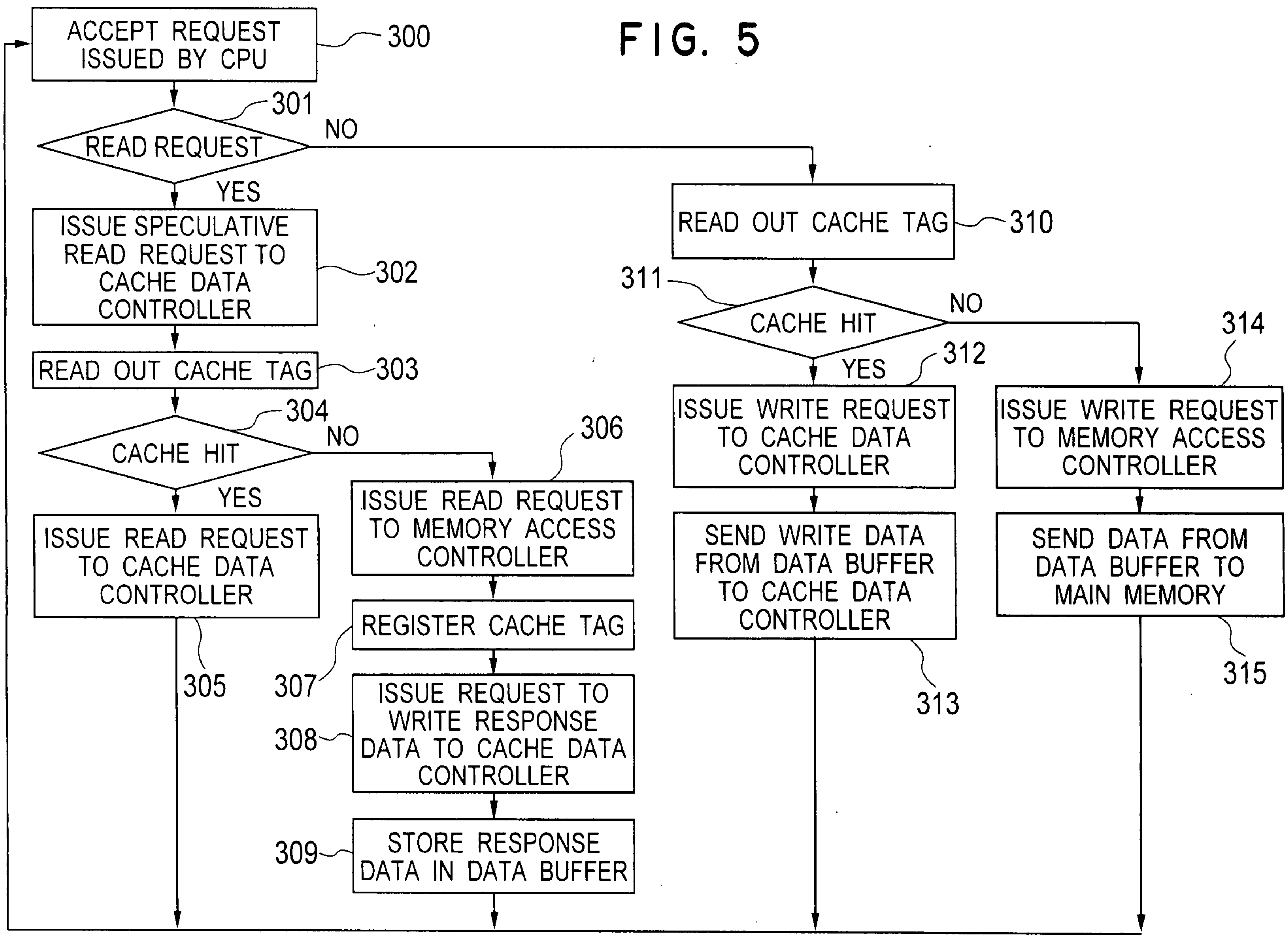

ACCEPT REQUEST ISSUED BY CPU
300
READ REQUEST
301
NO
YES
ISSUE SPECULATIVE READ REQUEST TO CACHE DATA CONTROLLER
302
READ OUT CACHE TAG
303
CACHE HIT
304
NO
YES
ISSUE READ REQUEST TO CACHE DATA CONTROLLER
305
ISSUE READ REQUEST TO MEMORY ACCESS CONTROLLER
306
REGISTER CACHE TAG
307
ISSUE REQUEST TO WRITE RESPONSE DATA TO CACHE DATA CONTROLLER
308
STORE RESPONSE DATA IN DATA BUFFER
309
READ OUT CACHE TAG
310
CACHE HIT
311
NO
YES
ISSUE WRITE REQUEST TO CACHE DATA CONTROLLER
312
SEND WRITE DATA FROM DATA BUFFER TO CACHE DATA CONTROLLER
313
ISSUE WRITE REQUEST TO MEMORY ACCESS CONTROLLER
314
SEND DATA FROM DATA BUFFER TO MAIN MEMORY
315

FIG. 6

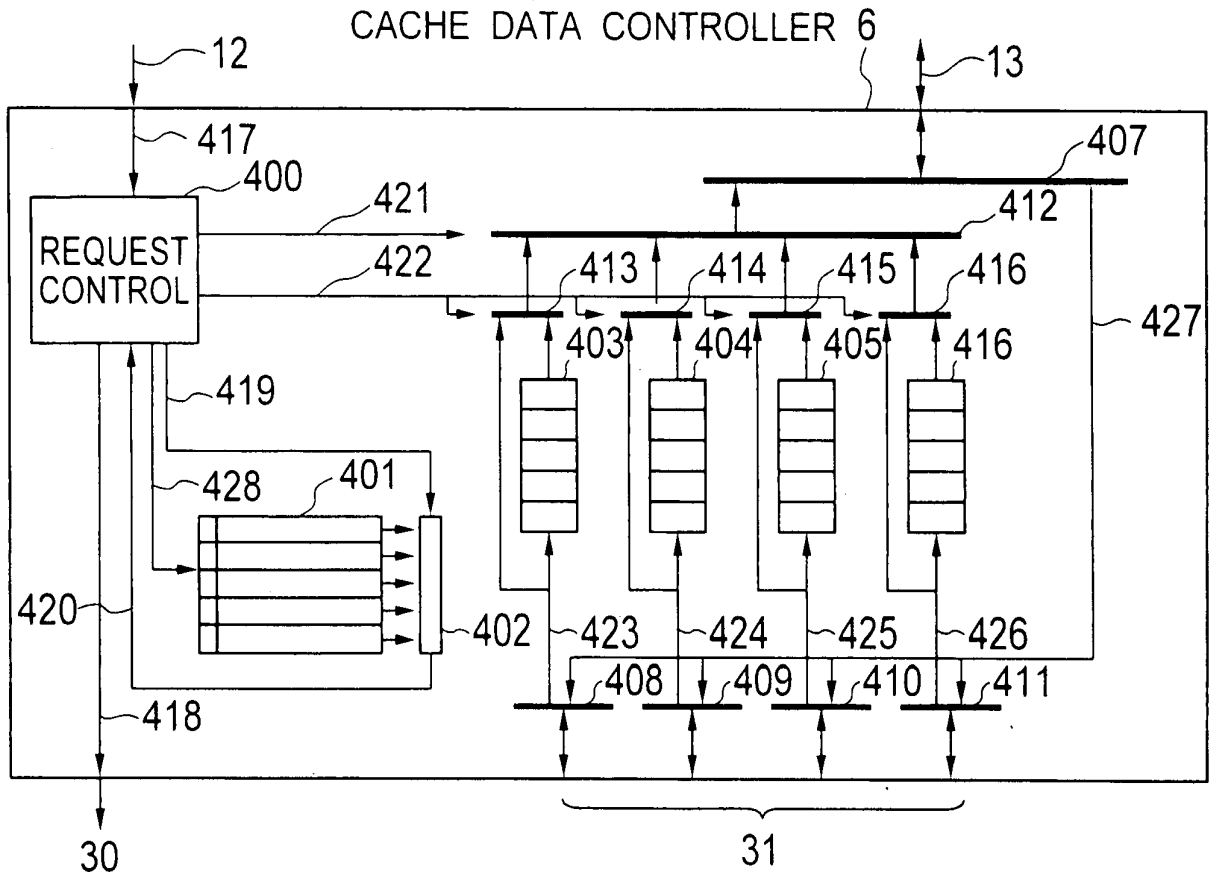

CACHE DATA CONTROLLER 6
12
13
417
400
407
421
412
REQUEST CONTROL
422
413
414
415
416
427
403
404
405
416
419
428
401
420
402
423
424
425
426
408
409
410
411
418
30
31

FIG. 7

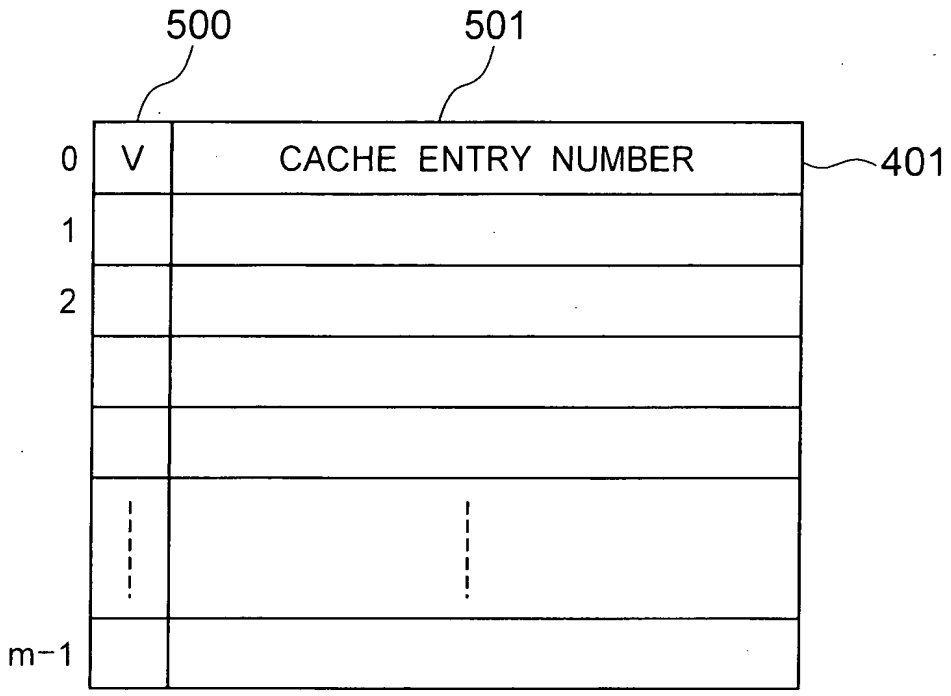

500
501
0
V
CACHE ENTRY NUMBER
401
1
2
m-1

FIG. 8

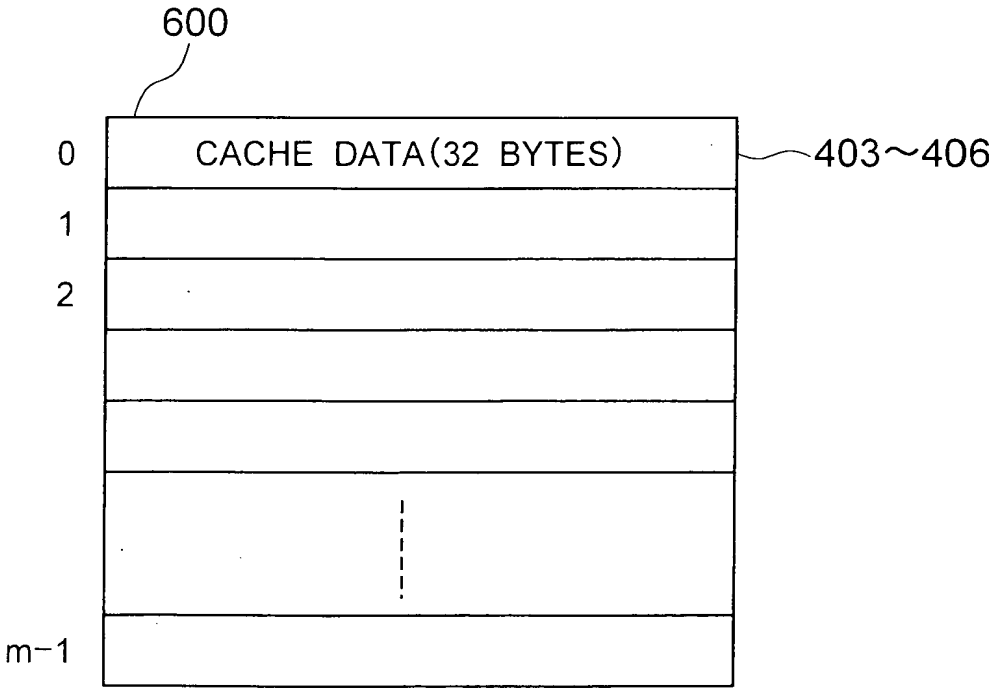
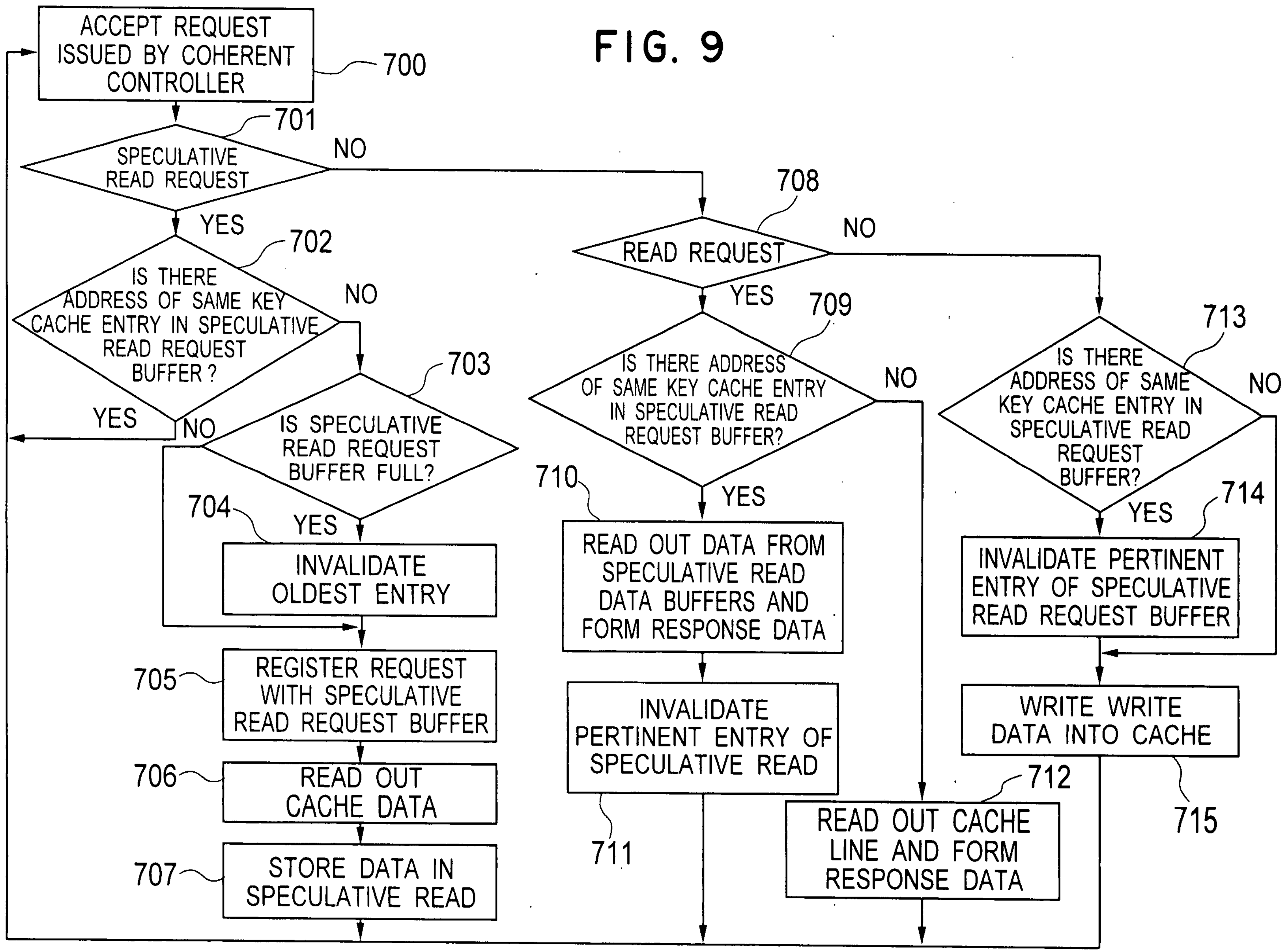

600
0
CACHE DATA(32 BYTES)
403~406
1
2
m-1

FIG. 9



ACCEPT REQUEST ISSUED BY COHERENT CONTROLLER
700
701
SPECULATIVE READ REQUEST
NO
YES
702
IS THERE ADDRESS OF SAME KEY CACHE ENTRY IN SPECULATIVE READ REQUEST BUFFER ?
NO
YES
NO
703
IS SPECULATIVE READ REQUEST BUFFER FULL?
YES
704
INVALIDATE OLDEST ENTRY
705
REGISTER REQUEST WITH SPECULATIVE READ REQUEST BUFFER
706
READ OUT CACHE DATA
707
STORE DATA IN SPECULATIVE READ
708
READ REQUEST
NO
YES
709
IS THERE ADDRESS OF SAME KEY CACHE ENTRY IN SPECULATIVE READ REQUEST BUFFER?
NO
YES
710
READ OUT DATA FROM SPECULATIVE READ DATA BUFFERS AND FORM RESPONSE DATA
INVALIDATE PERTINENT ENTRY OF SPECULATIVE READ
711
712
READ OUT CACHE LINE AND FORM RESPONSE DATA
713
IS THERE ADDRESS OF SAME KEY CACHE ENTRY IN SPECULATIVE READ REQUEST BUFFER?
NO
YES
714
INVALIDATE PERTINENT ENTRY OF SPECULATIVE READ REQUEST BUFFER
WRITE WRITE DATA INTO CACHE
715

FIG. 10

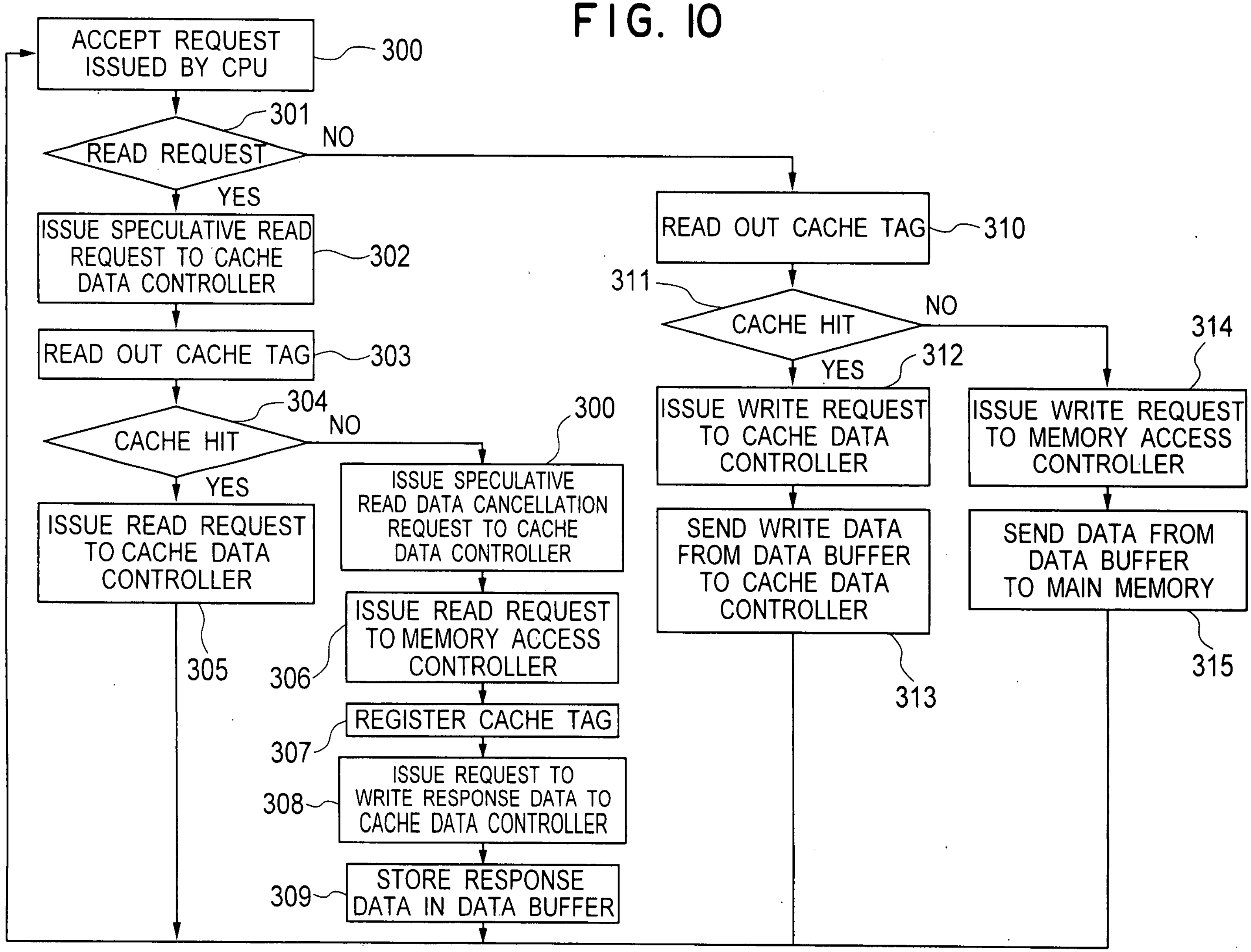
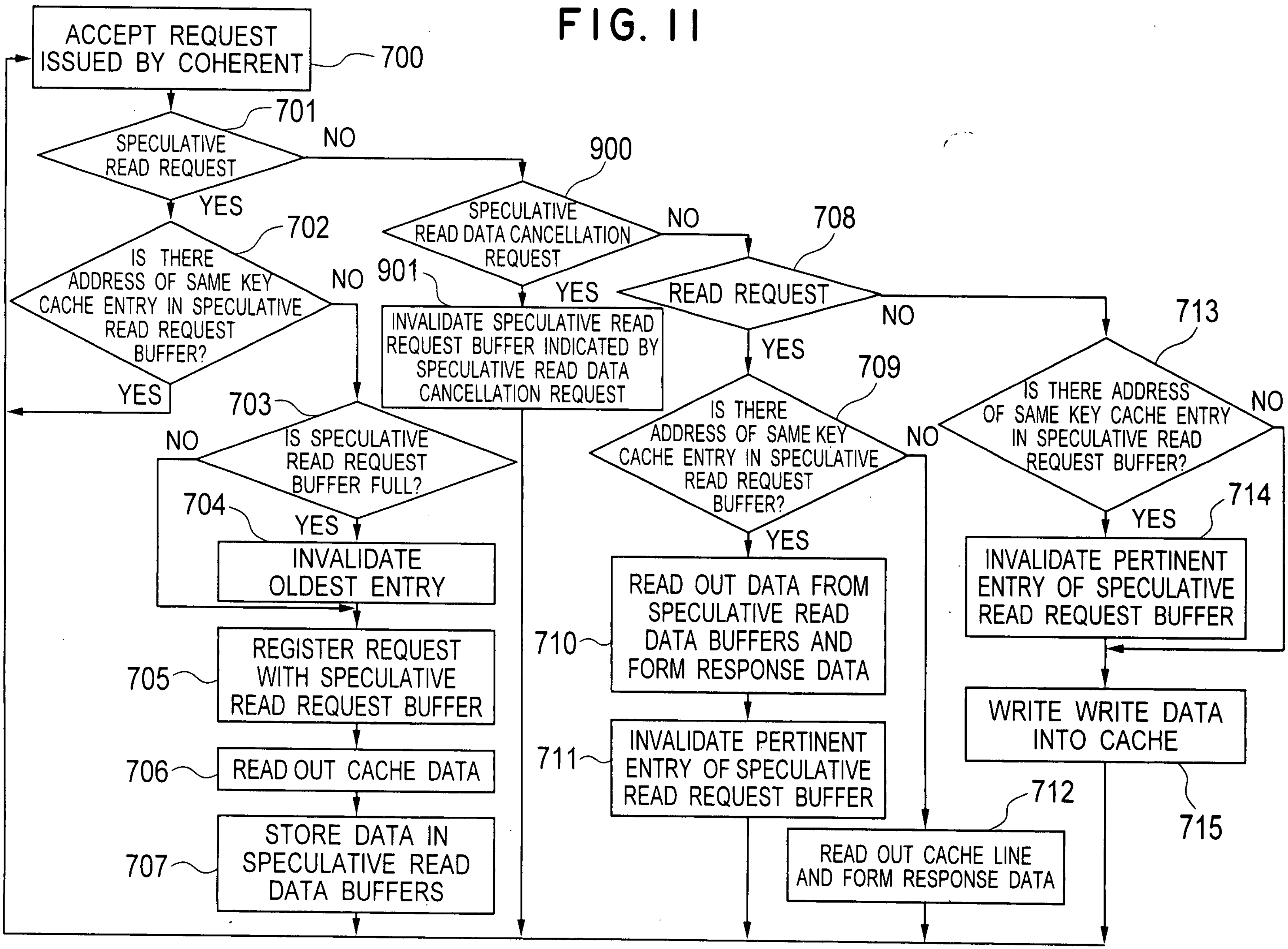
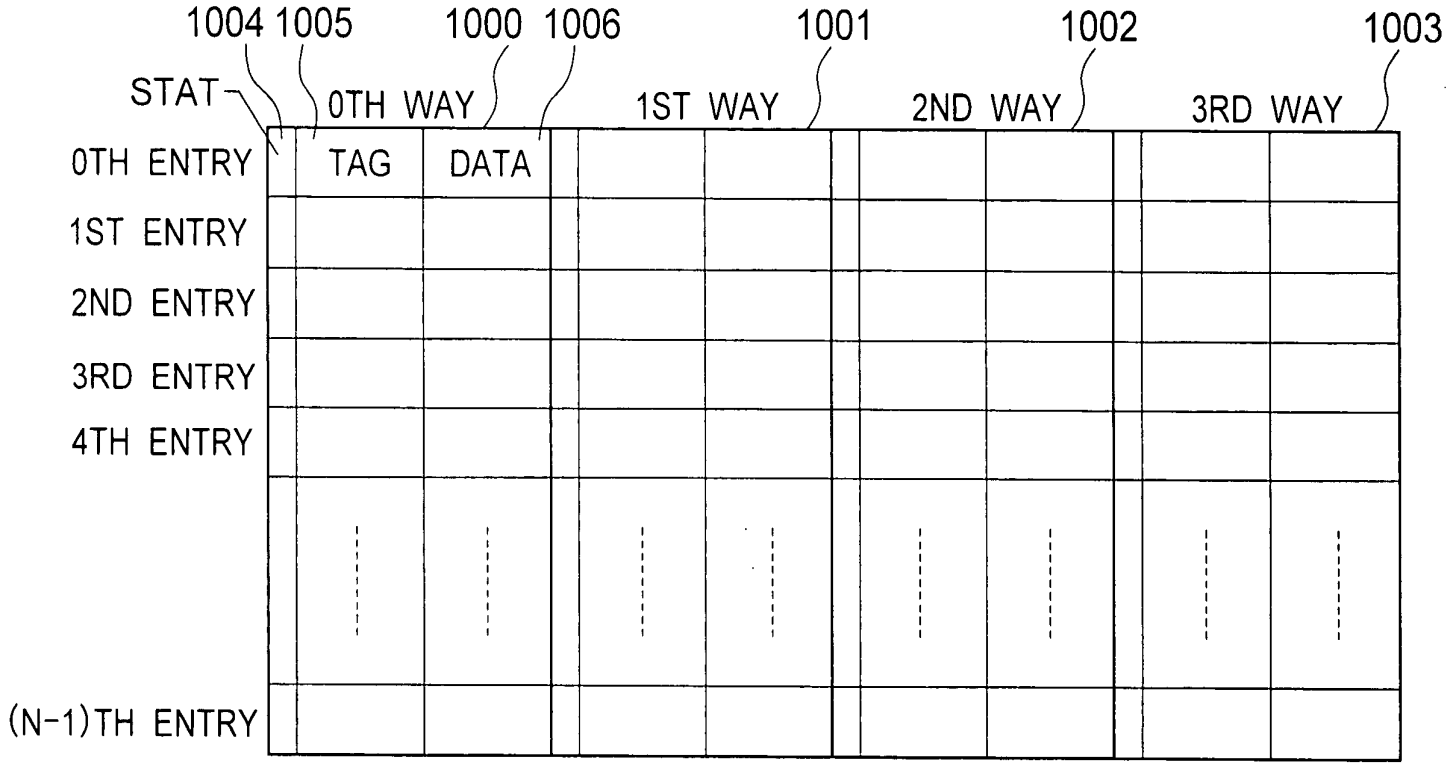

ACCEPT REQUEST ISSUED BY CPU
300
READ REQUEST
301
NO
YES
ISSUE SPECULATIVE READ REQUEST TO CACHE DATA CONTROLLER
302
READ OUT CACHE TAG
303
CACHE HIT
304
NO
YES
ISSUE READ REQUEST TO CACHE DATA CONTROLLER
305
ISSUE SPECULATIVE READ DATA CANCELLATION REQUEST TO CACHE DATA CONTROLLER
300
ISSUE READ REQUEST TO MEMORY ACCESS CONTROLLER
306
REGISTER CACHE TAG
307
ISSUE REQUEST TO WRITE RESPONSE DATA TO CACHE DATA CONTROLLER
308
STORE RESPONSE DATA IN DATA BUFFER
309
READ OUT CACHE TAG
310
CACHE HIT
311
NO
YES
ISSUE WRITE REQUEST TO CACHE DATA CONTROLLER
312
SEND WRITE DATA FROM DATA BUFFER TO CACHE DATA CONTROLLER
313
ISSUE WRITE REQUEST TO MEMORY ACCESS CONTROLLER
314
SEND DATA FROM DATA BUFFER TO MAIN MEMORY
315

FIG. 11



ACCEPT REQUEST ISSUED BY COHERENT
700
SPECULATIVE READ REQUEST
701
NO
YES
IS THERE ADDRESS OF SAME KEY CACHE ENTRY IN SPECULATIVE READ REQUEST BUFFER?
702
NO
YES
IS SPECULATIVE READ REQUEST BUFFER FULL?
703
NO
YES
INVALIDATE OLDEST ENTRY
704
REGISTER REQUEST WITH SPECULATIVE READ REQUEST BUFFER
705
READ OUT CACHE DATA
706
STORE DATA IN SPECULATIVE READ DATA BUFFERS
707
SPECULATIVE READ DATA CANCELLATION REQUEST
900
NO
YES
INVALIDATE SPECULATIVE READ REQUEST BUFFER INDICATED BY SPECULATIVE READ DATA CANCELLATION REQUEST
901
READ REQUEST
708
NO
YES
IS THERE ADDRESS OF SAME KEY CACHE ENTRY IN SPECULATIVE READ REQUEST BUFFER?
709
NO
YES
READ OUT DATA FROM SPECULATIVE READ DATA BUFFERS AND FORM RESPONSE DATA
710
INVALIDATE PERTINENT ENTRY OF SPECULATIVE READ REQUEST BUFFER
711
READ OUT CACHE LINE AND FORM RESPONSE DATA
712
IS THERE ADDRESS OF SAME KEY CACHE ENTRY IN SPECULATIVE READ REQUEST BUFFER?
713
NO
YES
INVALIDATE PERTINENT ENTRY OF SPECULATIVE READ REQUEST BUFFER
714
WRITE WRITE DATA INTO CACHE
715

FIG. 12


1004
1005
1000
1006
1001
1002
1003
STAT
0TH WAY
1ST WAY
2ND WAY
3RD WAY
0TH ENTRY
TAG
DATA
1ST ENTRY
2ND ENTRY
3RD ENTRY
4TH ENTRY
(N-1)TH ENTRY